UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,164	08/25/2000	Yih-Feng Chyan	15-6-9	6246

7590 10/22/2002

Lucent Technologies Inc
600 Mountain Avenue (Room 3C-512)
P O Box 636
Murray Hill, NJ 07974-0636

EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/648,164	Applicant(s) CHYAN ET AL.
	Examiner Thomas L Dickey	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *20-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-19* is/are rejected.

7)☒ Claim(s) *9 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 10 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The preliminary amendment filed on 07/06/98 has been entered.

Drawings

2. The formal drawings filed on 07/16/2002 are acceptable. 4 sheets were received, and have been entered in place of the 7 sheets originally filed, which have been cancelled.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 09/03/02 has been considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by UENISHI et al. (5,894,149).

Uenishi et al. discloses an integrated circuit structure comprising a semiconductor layer (parts 1,4, and 5 in common) having a major surface formed along a plane

(common surface of parts 4 and 5), first 4 and second (un-numbered "p" region in the center of figure 20) spaced-apart doped regions formed in the surface, a third doped region 5, over the first region 4 of different conductivity type than the first region 4, and a conductive layer 10 formed between the first and second regions and above the plane providing electrical connection between the doped regions, wherein the conductive layer 10 is a continuous film extending from the first region to the second region, which physically contacts the first region and the second region. Note figure 29 of Uenishi et al.

Claims 1-8, 10-13, and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by ISHIJIMA (4,920,397).

A. With regard to claims 1-4 and 10, Ishijima discloses an integrated circuit structure comprising a semiconductor layer 51 having a major surface formed along a plane 52, first 70 and second 68 spaced-apart doped regions formed in the surface, the first doped region 70 being a first source/drain region 70 of a MOSFET, the second region 68 being a portion of a transistor, to wit, a second source/drain region 68 associated with a second MOSFET, said structure further comprising a channel region of the second MOSFET aligned with the second source/drain region 68, a third doped region, being the upper portion of part 53, over the first region 70 of different conductivity type than the first region 70, the third region being a channel region 53 of the MOSFET, wherein the doped regions 70 and 68 are configured to form an inverter circuit, and a conductive layer 73 formed between the first 70 and second 68 regions and above the

plane 52 (note that portions of conductive layers 73 and 75 are formed above the plane, see figure 5, thus meeting the claim), providing electrical connection between the doped regions 70 and 68. Note figures 1 and 4-7, column 5 lines 45-69, and column 6 lines 1-59 of ishijima.

B. With regard to claims 1 and 5-8, Ishijima discloses an integrated circuit structure comprising a semiconductor layer 51 having a major surface formed along a plane 52, first 70 and second 68 spaced-apart doped regions formed in the surface, a third doped region, being the upper portion of part 53, over the first region 70 of different conductivity type than the first region 70, and a fourth doped region, being the upper portion of part 51, over the second region 68 of different conductivity type than the second region 68, a fifth doped region 76 over the fourth doped region 51 of the same conductivity type as the second region 68, a sixth doped region 78 over the third doped region 53 of the same conductivity type as the first region 70, said first 70, second 68, third 53, fourth 51, fifth 76 and sixth 78 regions and conductive layer 73 configured as two interconnected transistors, wherein one of the transistors is a MOSFET, the two transistors are of complementary conductivity type, and the transistors are configured to form an inverter circuit, and a conductive layer 73 formed between the first 70 and second 68 regions and above the plane 52, providing electrical connection between the doped regions 70 and 68. Note figures 1 and 4-7, column 5 lines 45-69, and column 6 lines 1-59 of ishijima.

C. With regard to claims 1 and 11-13, Ishijima discloses an integrated circuit structure comprising a semiconductor layer 51 having a major surface formed along a plane 52, first 70 and second 68 spaced-apart doped regions, being first and second source/drain regions, formed in the surface, a third doped region, being the upper portion of part 53, being a channel region 53, over the first region 70 of different conductivity type than the first region 70, a second channel region, being the upper portion of part 51, formed over the second source/drain region, third and fourth spaced-apart source/drain regions each vertically aligned with one of the channel regions 51 and 53 and one of the first 68 and second 70 source/drain regions, a conductive layer 73 formed between the first 70 and second 68 regions and above the plane 52, providing electrical connection between the doped regions 70 and 68, and a conductive element 64-65 connected to simultaneously control operation of both transistors, wherein the conductive element 64-65 is a continuous film extending from the first region 70 to the second region 68 comprising polysilicon and the transistors each include a gate contact region adjacent the channel region and connected to the conductive element 64-65, said transistors configured to form an inverter circuit function. Note figures 1 and 4-7, column 5 lines 45-69, and column 6 lines 1-59 of ishijima. For the continuous film and simultaneous control limitations note especially figure 7, which shows that gate electrodes 65 and 64 are formed from a continuous film controlling both transistors.

D. With regard to claims 15-18, Ishijima discloses an integrated circuit structure comprising a first layer 51 of semiconductor material, a first field effect transistor having

a first source/drain region 70 formed in the first layer 51, a channel region, being the upper portion of part 53, and a second source/drain region 78 formed over the channel region 53, a second field effect transistor having a first source/drain region 68 formed in the first layer 51, a channel region, being the upper portion of part 51, formed over the first layer and a second source/drain region 76 formed over the channel region 51, and a conductive layer 73 comprising a metal positioned between the first source/drain region 70 of each transistor to conduct current from one first source/drain region 70 to the other first source/drain region 68, a plurality of additional field effect transistors having first source/drain regions 71 and 69 formed in the first layer 51, channel regions, being the upper portion of part 51 and 53, and second source/drain regions 77 and 79 formed over the channel regions 51 and 53, the first and second transistors are connected to form a circuit (sub-circuit) and the first, second and additional transistors configured into a circuit, specifically, an SRAM circuit cell. Note figures 1 and 4-7, column 5 lines 45-69, and column 6 lines 1-59 of ishijima. For the SRAM limitation note especially figure 1 which schematically shows the circuit formed by connections 73 and 75.

Allowable Subject Matter

5. Claims 9 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7725 for regular communications and 703-308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-09560956.

TLD

08/2002

Minh Loan Tran
Primary Examiner